

Texas A&M University
College of Engineering
Computer Science Department

CPSC 321 Computer Architecture and Engineering
Spring Semester 2003
SYLLABUS

Instructor: Dr. Michael E. Thomadakis
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1 Course Information

1.1 Course Basics

CPSC 321 is an introductory course on computer organization and architecture. It examines in-depth the inner-workings of modern digital computer systems and the tradeoffs present at the *hardware-software interface*. It provides insights in the design process of complex hardware systems. A digital design background is considered fundamental and it is mandatory. This course includes a significant design component based on Hardware-Description Language modeling and simulation of a non-trivial RISC processor.

1.2 Course Details

The first part of the course investigates the design of Instruction Set Architectures (ISAs) focusing on application and system factors that shape the design choices. We focus on the MIPS processor and its assembly language. The next part focuses on the hardware design of a full-blown Arithmetic and Logic Unit (ALU). We use the Verilog Hardware Description Language (HDL) to develop a working model of an ALU. Subsequently, we discuss broader Data Path design issues, including registers, interconnection structures and clocking methodologies. The next part discusses Control Unit (CU) design, including hardwired and micro-programmed styles. This part studies the concept and mechanisms of machine exceptions and interrupts. We gradually develop data-paths and associated control units with higher performance, focusing on single-cycle, multi-cycle and finally pipe-lined designs. The Reduced Instruction Set Computers (RISC) are the main focus but Complex Instruction Set Computers (CISC) are compared and discussed as well.

Next we focus on memory design issues. We discuss typical problems and investigate mechanisms put into place in order to make the memory capable to support the instruction and data access rates of modern processors. We study both single and multi-level cache memories and a number of block placement, replacement and write policies. We then extend the memory hierarchy design with the study of virtual memories. We focus on single and multi-level page table and segmentation with paging and TLB designs.

Finally, we discuss processor–memory and I/O–processor inter-connections with various types of buses. Time permitting we will touch upon parallel processor architectures.

Several laboratory assignments will provide hands-on experience on MIPS assembly and the Verilog hardware description language, emphasizing structural and behavioral designs. The main material is complemented with actual system discussion. Projects allow students to implement material taught in the lectures and laboratory. We use processor simulators and the Verilog HDL as tools in our design and performance investigations. A sequence of design projects implements a subset of a realistic RISC architecture.

1.3 Official Course Site and Newsgroup

Visit often

- <http://courses.cs.tamu.edu/miket/cpsc321/> and,
- <news:tamu.classes.cpsc321>

for official announcements and up-to-the-minute information. **Visit often both sites.**

1.4 Course Catalog Description

Basic hardware/software components and the functional architecture of computers; syntax and semantics of a typical microprocessor assembly language; instruction sets, construction and execution of an assembly program; the design of I/O modules, memory, control unit and arithmetic unit.

1.5 Prerequisites

ELEN 248 or ELEN 220. Lab assignments will be done on UNIX and PC (windows) workstations and will require basic computer skills. Obtain accounts on both systems.

Main Textbooks

Required [PaHe1998] David. A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, Second Edition, Morgan-Kaufmann Publishers Inc. 1998, ISBN 1-55860-428-6. Publisher's URL:

http://www.mkp.com/books_catalog/catalog.asp?ISBN=1-55860-428-6.

Be sure to get the second edition of the text, **not** the first one. Other material will be referenced as needed.

Reference #1 [BroVra2003] Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design*, McGraw-Hill, 2003, ISBN 0-07-282315-1. Publisher's URL:

<http://higher.ed.mcgraw-hill.com/sites/0072823151/> This reference is strongly recommended.

Reference #2 [MMM2001] M. Morris Mano, *Digital Design*, 3rd Edition, Prentice Hall, Upper-Saddle River, New Jersey, 2002, ISBN 0-13-062121-8. Publisher's URL:

<http://vig.prenhall.com/catalog/academic/product/1,4096,0130621218,00.html> This is an alternative to [BroVra2003] above, but it lacks coverage of certain digital design and Verilog modeling topics.

Reference #3 [HePa2002] J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 3rd Edition, Morgan Kaufmann Publishers, Menlo Park, CA, 2002. We will occasionally use material from this more advanced text. It is a useful reference for those interested in pursuing a computer architecture career.

2 Course Topics and Reading Assignments

Students are required to read the main textbooks [PaHe1998, BroVra2003] and other assigned material as announced. It is highly recommended to be familiar with the material ahead of the corresponding lecture. This course will focus on the topics shown in Table 1, which may not be covered in this order, or not at all, if time does not permit it. Topics on digital design and Verilog will be announced in class as the needs arise.

Table 1: Course Topics and Corresponding Textbook Chapters

Topic	Chapter Number
— Introduction; The 5 components of a computer; Performance; Technology and Delay Modeling	Ch. 1, 2 (partially)
— Intro to Instruction Set Architecture (ISA) Design; MIPS ISA; Translation of High-Level C Constructs into MIPS; Assemblers, Object Code Generation, Linking and Executable Loading; Run-time Execution Environment	Ch. 3, App. A.
— Review of Digital-Logic Design for Combinational Circuits	App. B.
— Introduction to Hardware Description Languages (Verilog) and the Design–Simulation Process; Overview of Computer Arithmetic and ALU Design; Structural Designs in Verilog	Ch. 4
— Review of Digital-Logic Design for Sequential Circuits; Register-Transfer Level Description of Systems	App. B.
— Single-Cycle Datapath and Control; Multi-cycle Datapath and Control; Microprogramming and Hard-wired Control Units; Behavioral HDL Description of Systems; Exceptions Handling	Ch 5, App. C
— Intro to Pipelining; Pipelined MIPS Datapath; Pipeline Hazards: Structural, Control, Data; Hazard Detection and Resolution; Pipelining control; Exceptions Handling	Ch. 6
— Overview of SRAM and DRAM Design; Memory Hierarchy; Cache memory design	Ch 7
— Virtual memory	Ch 7
— Buses, I/O Sub-systems, I/O Devices (selected topics)	Ch 8

3 Grading Scheme and Course Requirements

3.1 Attendance Policy

Class attendance is strongly recommended. The student is responsible for any material missed. Material covered in the lectures may not be found in the textbook or the transparencies. Missed exams and quizzes may be made

Table 2: Course Requirements and Corresponding Weight

1	Three / five mini-projects	30%
2	Several lab assignments	10%
3	HW assignments	05%
3	2 mid-term exams	30%
4	A final exam	25%

Table 3: Grading Brackets, V is your effective class average

$V \geq 90$	A
$80 \leq V < 90$	B
$70 \leq V < 80$	C
$60 \leq V < 70$	D
$V < 60$	F

up only when the absence is university sanctioned. Medical reasons or other extenuating conditions beyond the control of the student, must be properly documented. In general the student must discuss problems **before** the time of the examination and arrange for approval by the Instructor.

3.2 Grading Scheme

The course consists of lectures, reading, homework, lab assignments, projects and examination periods. The weights and the grade brackets are shown in Table 2 and 3, respectively.

3.3 Examinations

All major examinations will be held in class with exact dates determined in class. The exams will generally test your knowledge of assignment material, so you are responsible for mastering **all** lab, homework, and project material submitted with other partners, as if you did all the work by yourself. All exams will be closed book and closed notes (unless otherwise stated). The nature of the course material is such that the final exam must be cumulative.

3.4 Assignments

Projects are substantial assignments that will typically require about two to four weeks each to complete. There will be three to five projects, each carried out by a group of two to four people. You are encouraged to form groups as early as possible. Labs are intended to prepare you to tackle the projects, and you will typically be able to complete labs during the assigned lab period. Written lab work will be accepted up to the beginning of the following lab period. To obtain credit for a lab you typically must obtain a “check-off” from your lab instructor (TA), signifying that you completed the work during the scheduled lab time. You are responsible for attending lab and demonstrating to your lab instructor that you completed the work.

Homework will be assigned sporadically and will typically consist of end-of-chapter exercises and other problems. Homework exercises can be carried out by one or two people, unless stated otherwise.

Course labs and projects will involve programming in MIPS assembly language using the SPIM simulator, and solving problems in computer organization and design using the Verilog hardware description language. All tools run on departmental UNIX and Windows-PC systems, so you will need to get a student computer account immediately.

Assignment handouts will be placed on the course web page ahead of time. The correct approach is to start working on assignments as early as possible and contact us when you encounter difficulties. In general, the closer to the deadline you request our assistance, the harder may be to obtain our help.

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3.5 Deadline Policy

Late work will not be accepted, in general. Turn in all work by the established deadline. In case you have difficulties finishing an assignment contact the TA or the Instructor before the deadline. Late work can be accepted only under circumstances beyond student's control and after arrangement with the Instructor, prior to the deadline. **Note:** work turned-in on time is eligible for partial credit. It will always be better to turn work in by the deadline, as trying to "perfect" it and turn it in late will give you no points at all.

3.6 Submission of Work

All assignments deliverables must be submitted electronically, by the due date, using the `turnin` method. Late assignments are not going to be accepted in general, unless a University sanctioned excuse is provided ahead of time. A student will earn points when he/she submits the assignment on time, by the partial credit policy. Note that **email** submissions will not be accepted (they will be ignored without notice). You have to follow the submission and media policies and guidelines published on the web.

3.7 Re-grading Policy

A student can request re-grading of assignments and exams, if he/she believes that the points assigned are inconsistent with the quality and merits of the submitted work. To request re-grading you have to follow the guidelines below.

1. Re-grading requests must be submitted AT MOST ONE WEEK AFTER the item has been graded and returned to the student and solutions have been made public. After this time limit NO re-grading requests will be honored.
2. Re-grading requests must be as specific as possible and must be accompanied by a reasonable amount of justification and documentation. Requests must be in written form for major assignments and exams.
3. E-mails must be sent to TAs and graders or the instructor within the one week time limit.

3.8 Excused Absences and Make-up Policy

Make-ups for assignments and exams will be given only under circumstances beyond student's control (*a university sanctioned excuse*). Prior arrangements with the instructor must be made when feasible and official verification of circumstances necessitating the absence will be required.

3.9 Group Work

Each assignment will state the number of people who can work together in a group. Some assignments will be done by students individually. Partners will turn in a single assignment paper (with each partner's name and section number on it) and each partner will receive the same grade. You are also free to work individually.

4 Teaching Personnel and Resources

The Instructor and the Teaching Assistants are your most valuable resource. We are available during our published office hours or at other times by appointment. Walk in any time during the office hours to see the instructor or the TAs. We can meet at other times but students need to arrange for an appointment. Unannounced visits outside office hours may not be honored. Make it a habit of yours to discuss with your TA or the Instructor homework problems and other assignments. Contact the TAs or the Instructor to collect your scores of all graded items. Observe the re-grade period mentioned above.

The Instructor and the TAs will provide all necessary resources for the course to progress smoothly, including, handouts, notes, programming code files, among others. Most items are posted to the web page for the students to down-load.

People having difficulties with either the material or finishing assignments, are strongly encouraged to discuss the problems with the Instructor and the TAs *as early as possible*. Things can be corrected when problems are addressed early. The Instructor will propose a recovery plan for the student. The recovery plan is a course of action that will assist the student boost his understanding of the material and perform better. As a rule of thumb, the more a student delays to contact the Instructor concerning problems with the material, the more intense effort will be required of the student in order to recover.

5 Scholastic Dishonesty

Plagiarism is the passing of someone else's work as one's own, without giving the original author due credit. Scholastic dishonesty will be treated very strictly as per Texas A&M University rules. Typically, the given incidence **has to be reported to the Department Head**. The Department Head will then determine the type of punitive actions, including, 0 points to the assignment, an F grade in the course, academic suspension, or even expulsion from Texas A&M University.